Figures

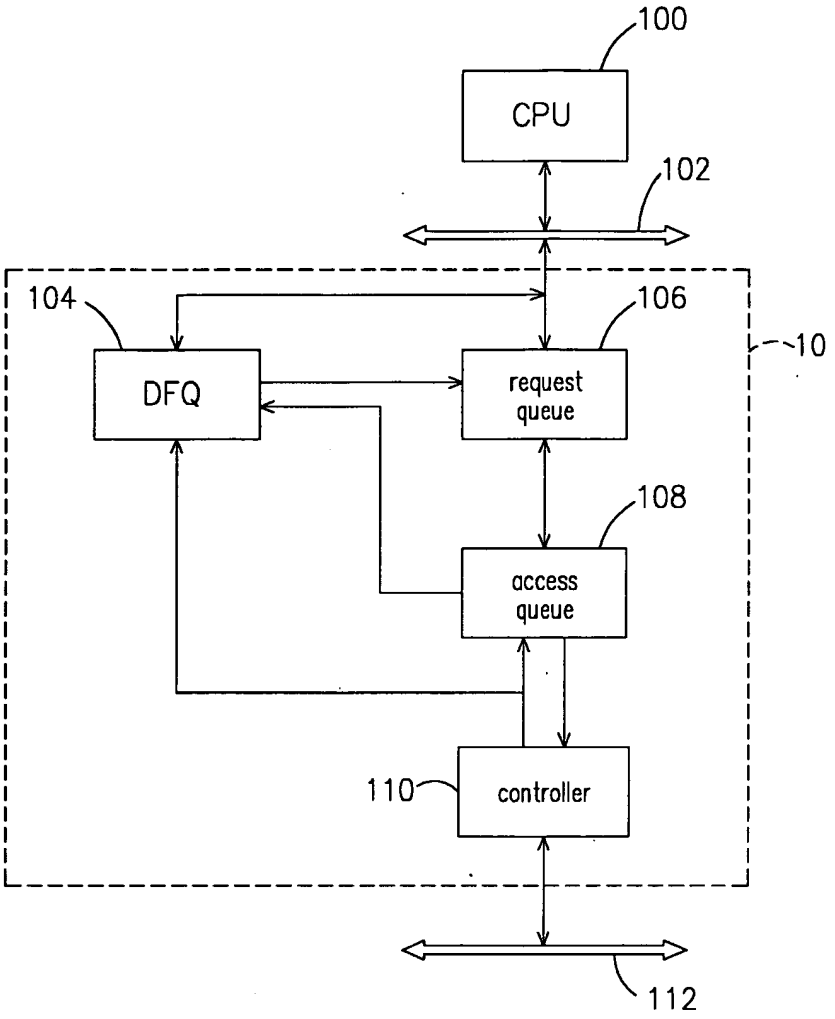
100
CPU
102
104
106
10
DFQ
request queue
108
access queue
110
controller
112

FIG. 1

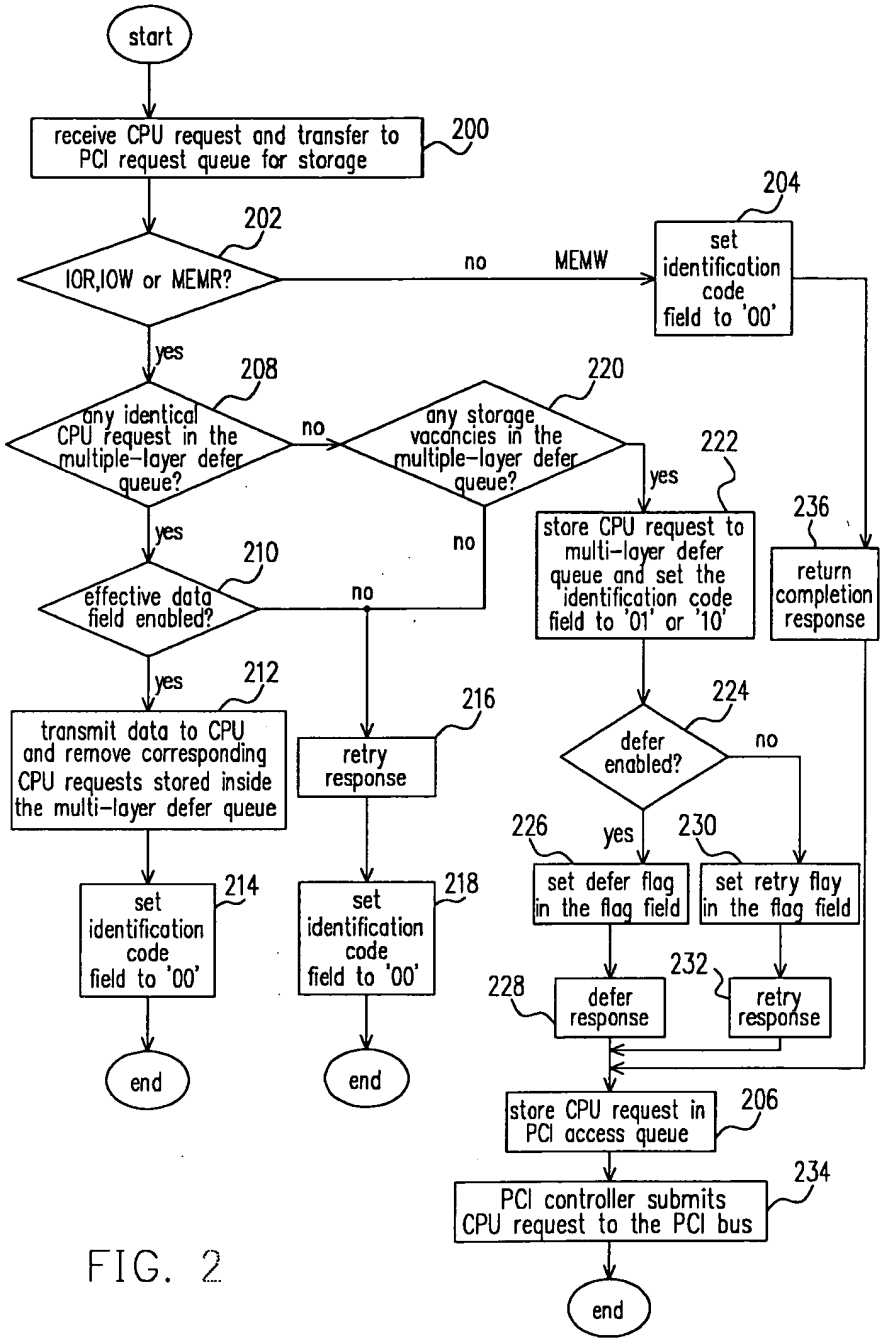
start
receive CPU request and transfer to PCI request queue for storage
200
IOR,IOW or MEMR?
202
no
MEMW
set identification code field to '00'
204
yes
any identical CPU request in the multiple-layer defer queue?
208
no
any storage vacancies in the multiple-layer defer queue?
220
yes
store CPU request to multi-layer defer queue and set the identification code field to '01' or '10'
222
return completion response
236
yes
effective data field enabled?
210
no
no
yes
transmit data to CPU and remove corresponding CPU requests stored inside the multi-layer defer queue
212
retry response
216
defer enabled?
224
no
yes
226
230
set defer flag in the flag field
set retry flay in the flag field
set identification code field to '00'
214
set identification code field to '00'
218
228
defer response
232
retry response
end
end
store CPU request in PCI access queue
206
PCI controller submits CPU request to the PCI bus
234
end

FIG. 2

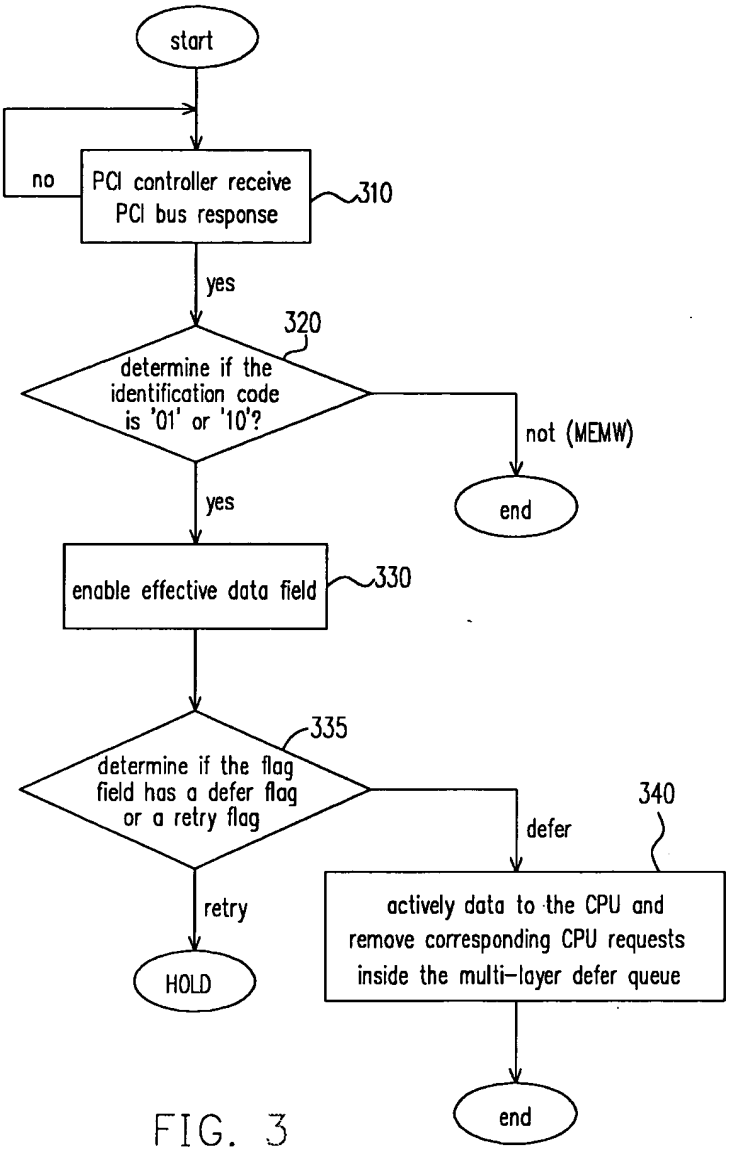
start
no
PCI controller receive PCI bus response
310
yes
320
determine if the identification code is '01' or '10'?
not (MEMW)
end
yes
enable effective data field
330
335
determine if the flag field has a defer flag or a retry flag
340
defer
retry
HOLD
actively data to the CPU and remove corresponding CPU requests inside the multi-layer defer queue
end

FIG. 3